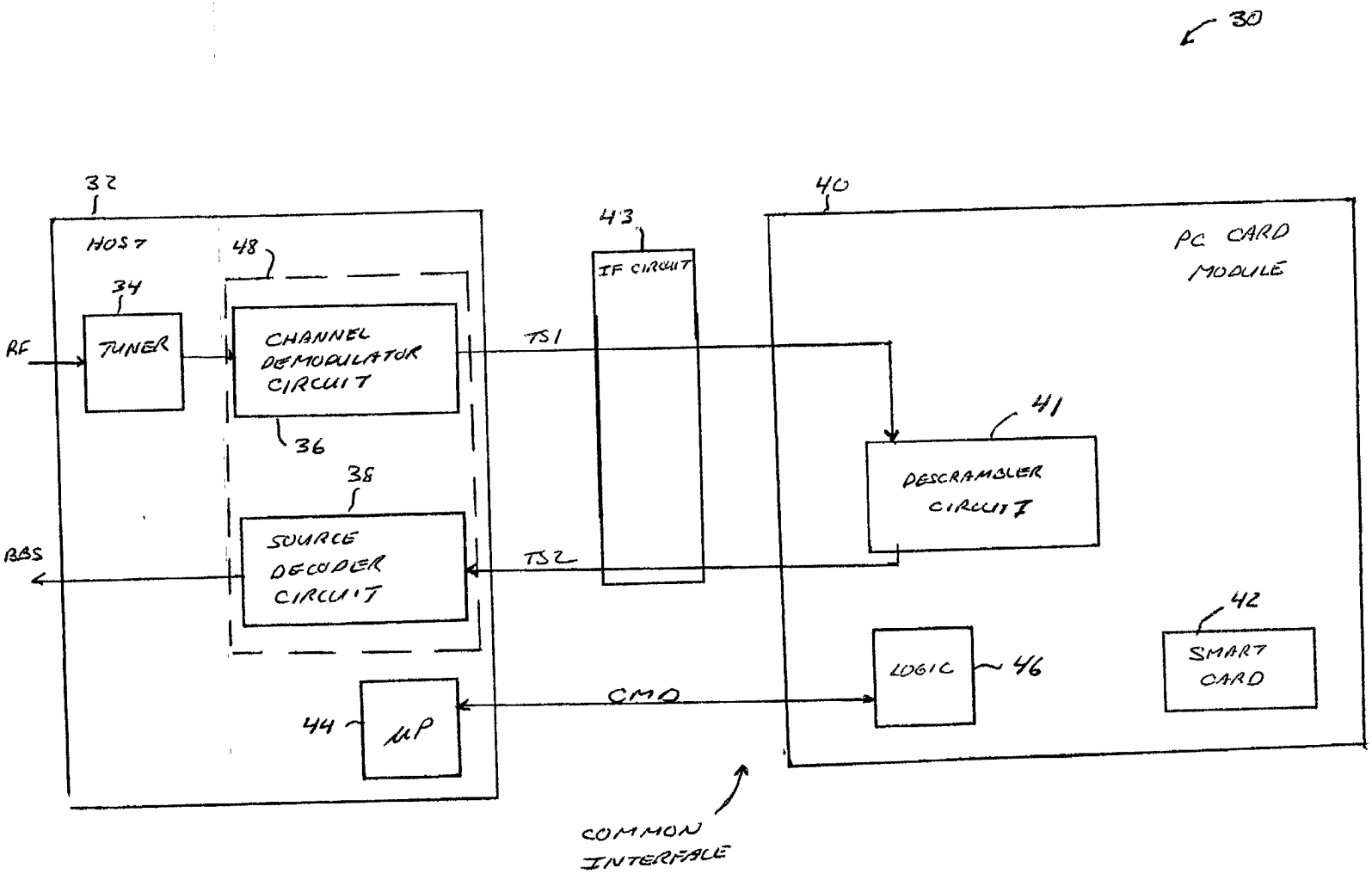


FIG. 1

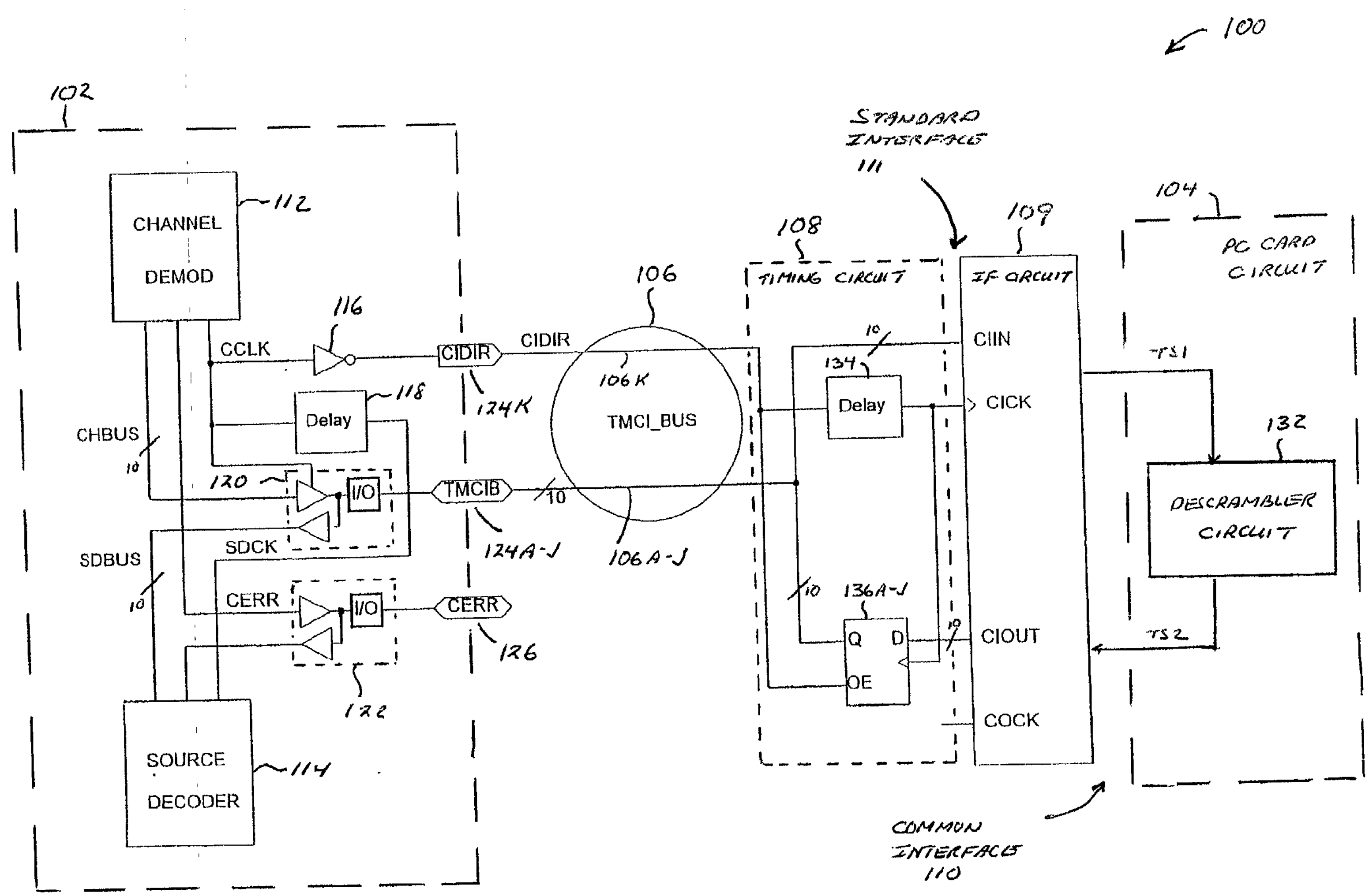

100
102
CHANNEL
DEMOD
112
116
CCLK
CIDIR
CIDIR
106
106K
TMCI_BUS
Delay
118
124K
CHBUS
10
120
I/O
TMCIB
10
SDCK
124A-J
106A-J
SDBUS
10
CERR
I/O
CERR
126
122
SOURCE
DECODER
114
STANDARD
INTERFACE
111
108
TIMING CIRCUIT
10
134
Delay
10
136A-J
Q
D
OE
10
109
IF CIRCUIT
CIIN
CICK
CIOUT
COCK
104
PC CARD
CIRCUIT
TS1
132
DESCRAMBLER
CIRCUIT
TS2
COMMON
INTERFACE
110

FIG. 2

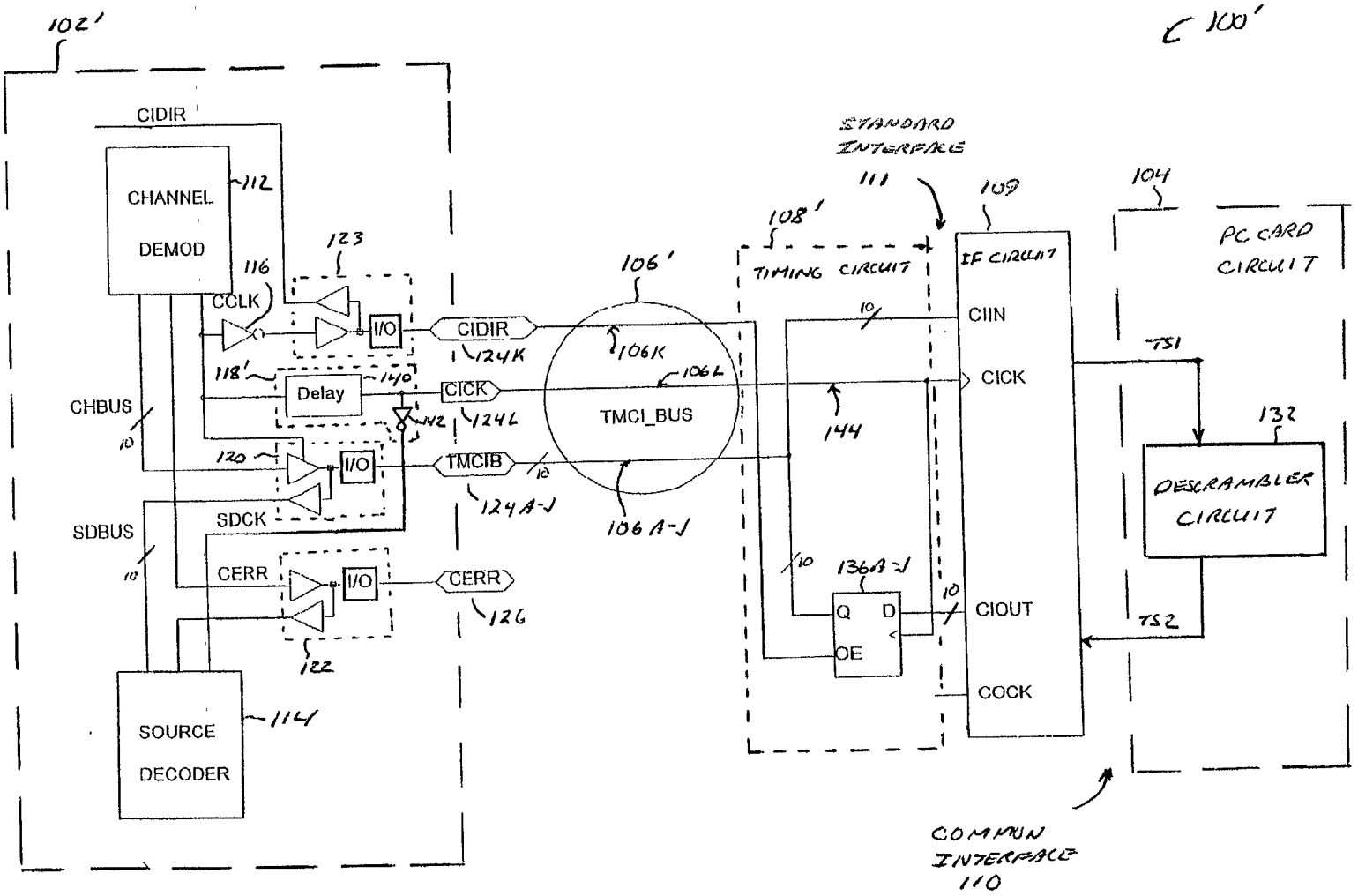


FIG. 3

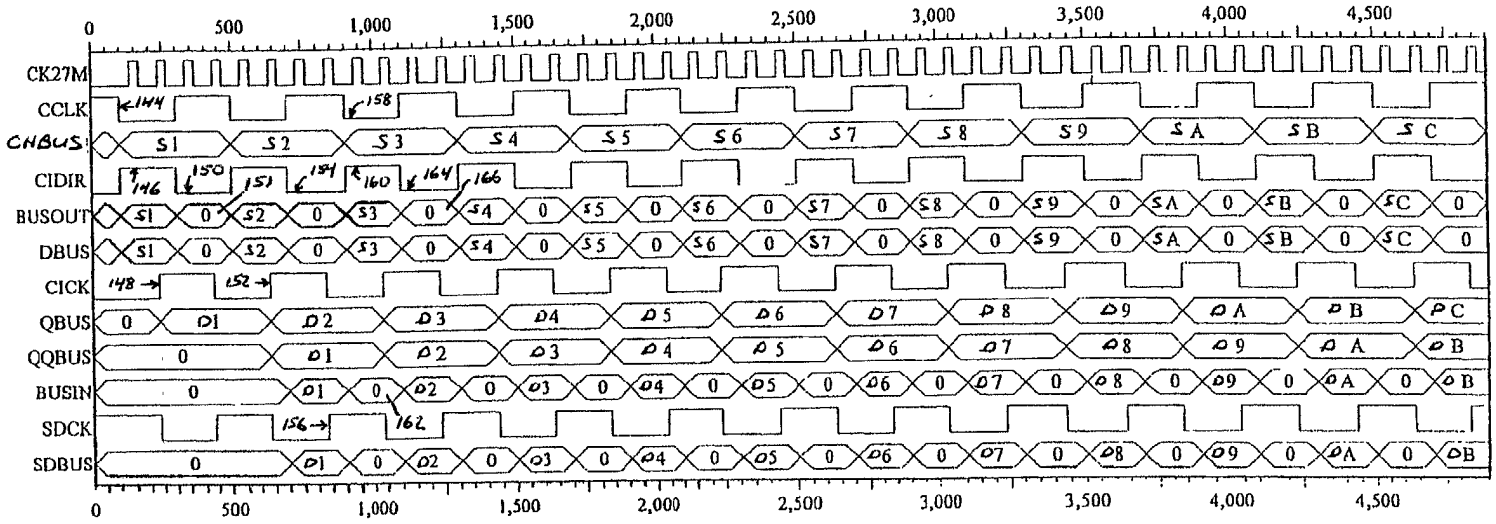
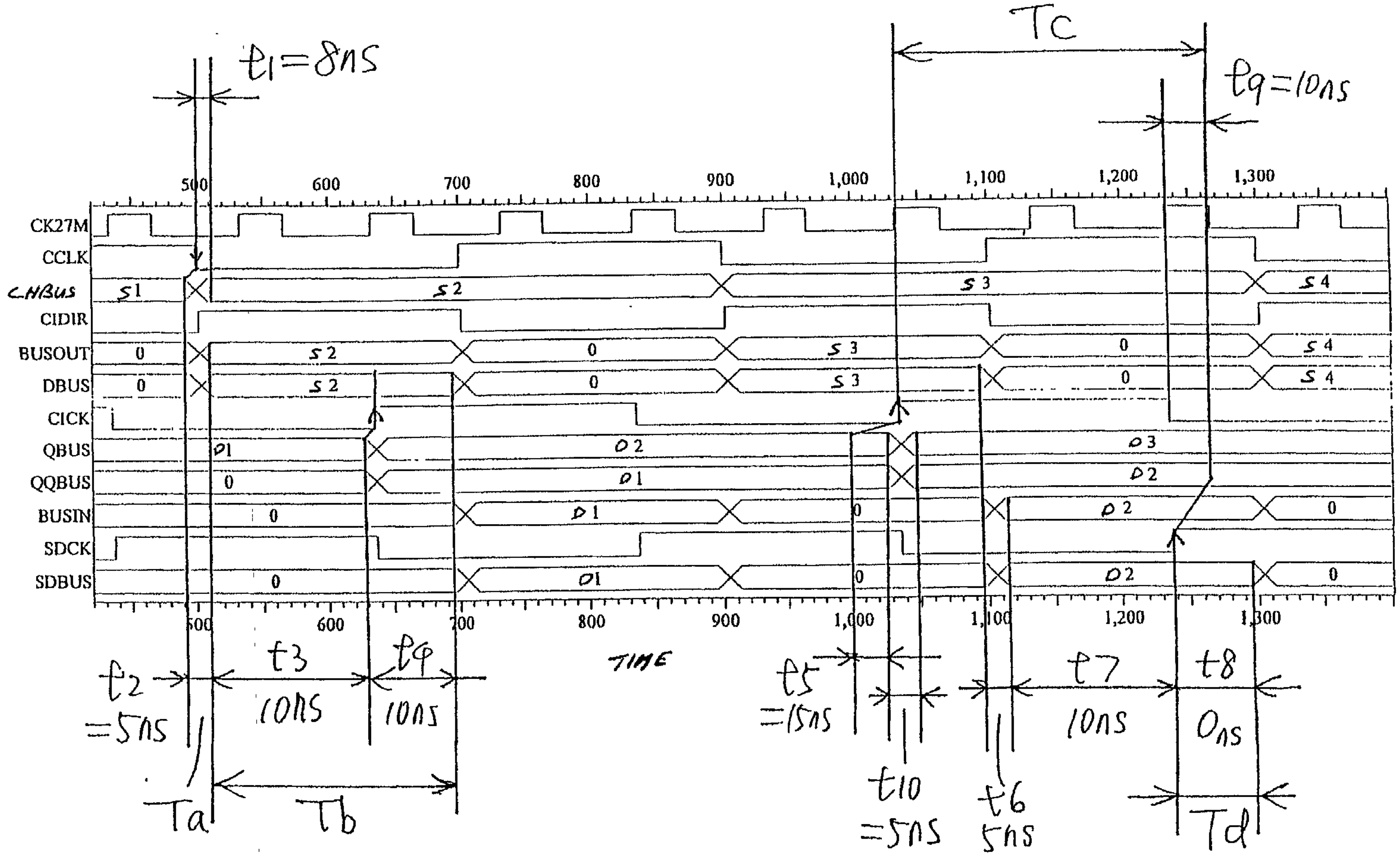


FIG. 4



CK27M
CCLK
CHBUS
CIDIR
BUSOUT
DBUS
CICK
QBUS
QQBUS
BUSIN
SDCK
SDBUS
TIME
t1=8ns
t2 =5ns
t3 10ns
t4 10ns
t5 =15ns
t6 5ns
t7 10ns
t8 0ns
t9=10ns
t10 =5ns
Ta
Tb
Tc
Td

FIG. 5